



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,918	12/03/2001	Neil Gibson	TI-32968	7227

7590 03/21/2003

Dan Swayze
Texas Instruments Incorporated
P.O. Box 655474
M/S 3999
Dallas, TX 75265

EXAMINER

NGUYEN, LINH V

ART UNIT	PAPER NUMBER
----------	--------------

2819

DATE MAILED: 03/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/008,918

Applicant(s)

GIBSON ET AL.

Examiner

Linh V. Nguyen

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-19 is/are allowed.
- 6) ☒ Claim(s) 1, 3-9, 20-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Response to Amendment

1. This office action is in response to applicant's amendment received on 1/17/03.

Claim 2 has been canceled. Claims 1, and 3 - 22, are pending on this application.

Response to Arguments

2. Regarding to claim 1, Under the "Remark", Applicant's argued that Uscategui amplifier circuit does not disclose g_m . Examiner respectfully traversed from the following: element g_m is a gain value, and the gain value is inherently in all model of all transistors amplifier circuit.

Regarding to claims 9, 20 and 22, Under the "Remark", applicant argued that Uscategui does not teach the plurality of transistor configured as translinear loop of the claimed invention. Examiner is respectfully traversed from the following:

Applicant's claimed invention fails to distinct the structures and limitation of the translinear loop over the references applied against the claims. Also Applicant needs to disclose or explain how the structures or limitation of the translinear loop of the claim avoid from the references or distinguish from them, and not because of the terminology of translinear loop.

Regarding to applicant's argued that the rejection under 35 U.S.C. 101 is premature since no application in fact patented or allowed. Examiner respectfully traversed because the rejection 35 U.S.C 101 is a **provisional** double patenting rejection since the conflicting claims have not in fact been patented.

Double Patenting

3. Claims 1, and 3 – 6, of this application conflict with claims 1 - 5 of Application No. 10005463. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

4. Claims 1 and 3 - 6, provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 – 5, of copending Application No. 10005463. This is a **provisional** double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3 – 9, 20 - 22, are rejected under 35 U.S.C. 102(b) as being anticipated by Uscategui et al. U.S. patent No. 5,789,982.

Fig. 2 Uscategui et al. clearly disclose an amplifier having: a pre-driver sub-stage and a final sub-stage, the pre-driver sub-stage (14) having a plurality of transistors

Art Unit: 2819

being biased by a plurality of current sources (current mirror (Q5 – Q6, Q8-Q9)), the pre-driver sub-stage being adapted to accept a current signal from an input gm cell (Q1 – Q4 [element gm is a gain value, and the gain value is inherently all model of amplifier circuit]); the pre-driver stage being further adapted to provide biasing to a plurality of transistors (Q13, Q14) in the final sub-stage (16); and the pre-driver sub-stage being coupled to the final sub-stage (Q13, Q14) so as to provided current gain from input to output of $I_{out} = B_n \cdot B_p \cdot I_{in}$ (inherent from beta gain of each transistor); and localized feedback circuitry enclosed in the output stage (Col. 1 lines 9 – 12), operable to correct signal errors more rapidly than an overall amplifier feedback loop (this is a improving statement only, because it does not teach any structures or limitation of the present invention), thereby improving the speed characteristics of the operational amplification output stage (this is a improving statement only, because it does not teach any structures or limitation of the present invention).

7. Regarding to claim 3, wherein the localized feedback comprising inherent RHPZ cancellation operable to extend bandwidth (As applicant stated, “ RHPZ cancellation operable to extend bandwidth is inherent to the structure of claim 1 invention. Therefore RHPZ must be inherent to Uscategui et al as applied to claim 1 above, also.) .

8. Regarding to claim 4, wherein the plurality of transistors in the final sub-stage comprises 4 transistors (Q13, Q14) arranged as a complementary pair of differential transistors.

9. Regarding to claim 5, the operational amplifier output stage recited in use in an integrated circuit (Abstract).

10. Regarding to claim 7, wherein the pre-driver sub-stage comprises two circuits, the first pre-driver sub-stage (top 26, Q15) circuit being adapted to condition a positive portion inputted signal for transfer to a first final sub-stage circuit (Q13) of the final sub-stage, and the second pre-driver sub-stage (bottom 26, Q16) circuit being adapted to condition a negative portion of an inputted signal for transfer to a second final sub-stage (Q14) circuit of the final sub stage;

11. Regarding to claim 8, wherein the first final sub-stage circuit and the second final sub-stage circuit are interconnected at an output terminal node (32) such that the conditioned and amplified positive portion the signal and the conditioned and amplified negative portion o t the signal are joined in phase with minimal crossover distortion the output signal having the form $I_{out} = B_n * B_p * I_{in}$ (inherent from beta gain of each transistor).

12. Regarding to claim 9, 20 - 22, the amplifier claimed device and method are deemed to be made clearly inherent by the amplifier of Uscategui et al. as applied to claim 1, 3 – 5, 7, and 8 above. (Hence the claimed invention fails to teach the structures or limitation for configuration of transistors in translinear loop over the reference applied to the claim)

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2819

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uscategui et al., in view of Applicant Admitted Prior Art (AAPA).

The amplifier of Uscategui et al. as applied to claims 1 – 4 above, disclose every aspect of applicant's claimed invention except not explicitly disclose the amplifier is use in a DSL driver. However, in DSL application, using amplifier is a well-known art and conventional as AAPA has disclosed in the background of the invention. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to apply the amplifier of Uscategui et al in DSL application for the purpose of reduction harmonic distortion in amplifier circuit (Uscategui Col. 1 line 23 –13).

Allowable Subject Matter

15. Claims 10 – 19, are allowed.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

Art Unit: 2819

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

March 19, 2003


Michael Tokar
Supervisory Patent Examiner
Technology Center 2800